10

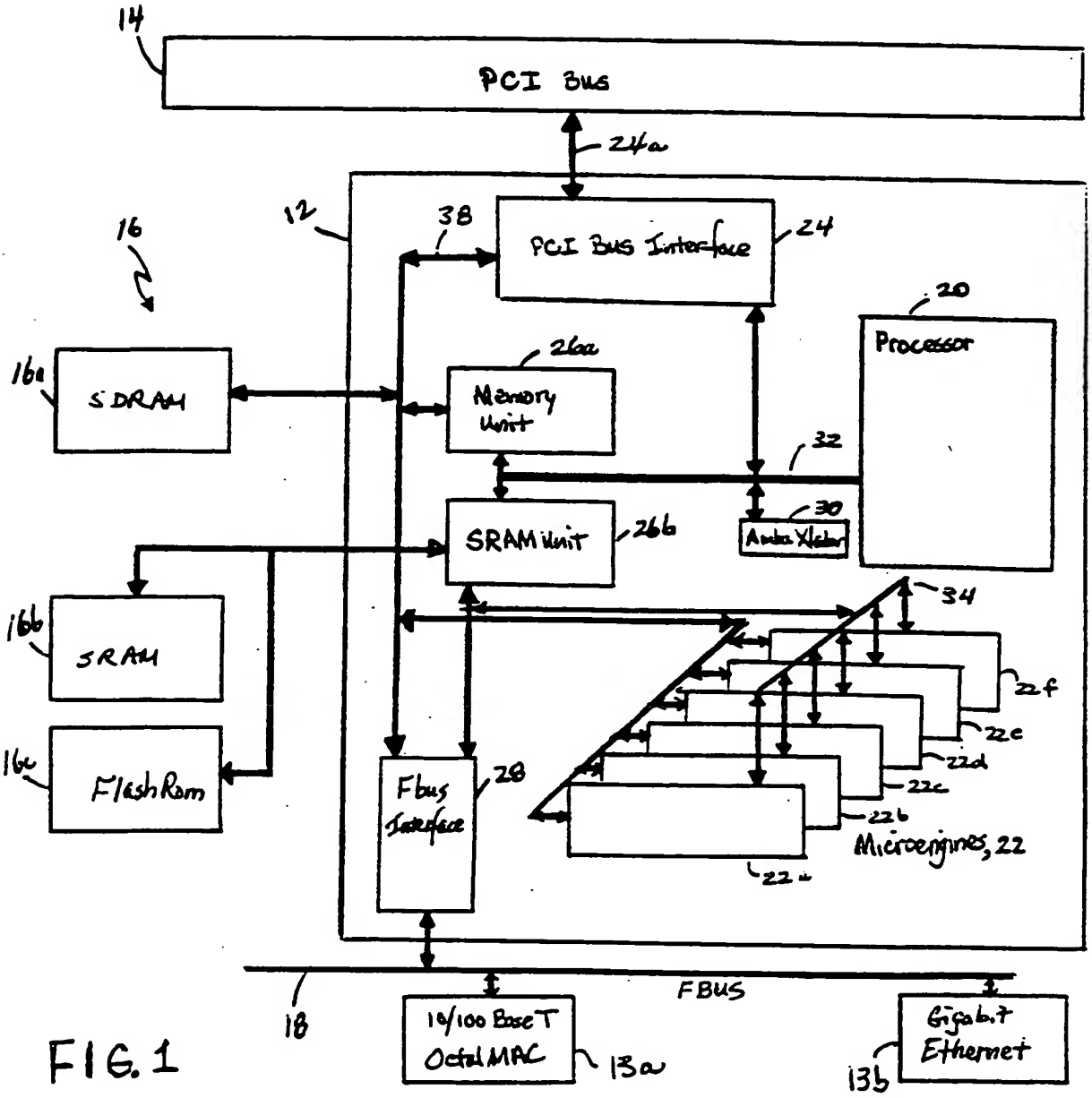

14
PCI Bus
24a
12
38
PCI Bus Interface
24
16
20
Processor
16a
SDRAM
26a
Memory Unit
32
30
Arbiter
SRAM Unit
26b
34
16b
SRAM
22f
22e
22d
22c
22b
22a
Microengines, 22
16c
Flash Rom
Fbus Interface
28
FBUS
18
10/100 BaseT Octal MAC
13a
Gigabit Ethernet
13b

FIG. 1

10/070006

WO 01/16758

PCT/US00/23982

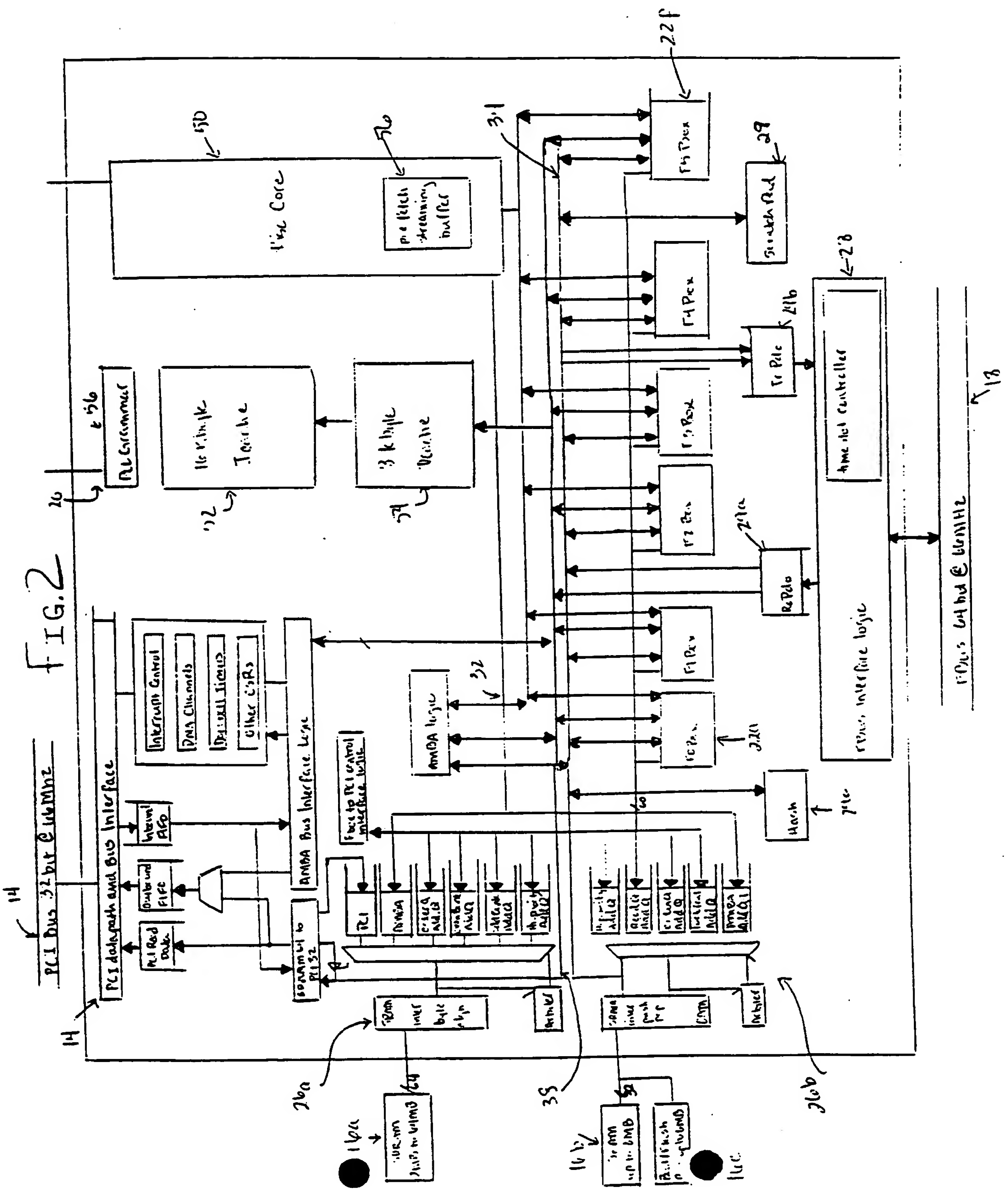


FIG. 2

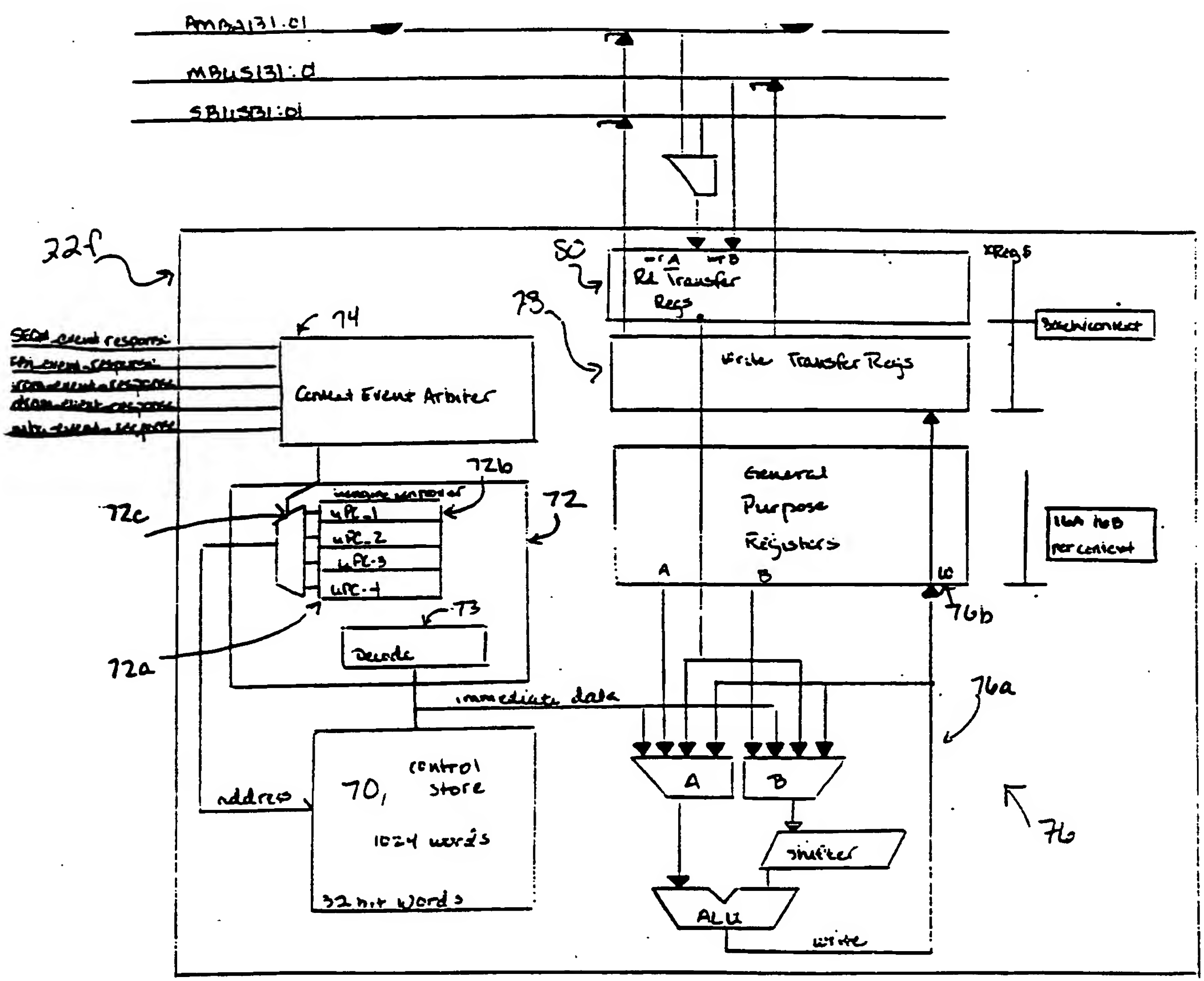

AMBA[31:0]
MBUS[31:0]
SBUS[31:0]
22f
80
Rd Transfer Regs
XRegs
78
Write Transfer Regs
74
Context Event Arbiter
72b
72
72c
uPC-1
uPC-2
uPC-3
uPC-4
73
Decode
72a
General Purpose Registers
A
B
W
76b
16A 16B per context
immediate data
76a
A
B
control store
70
1024 words
32 bit words
address
shifter
ALU
write
76

Fig 3

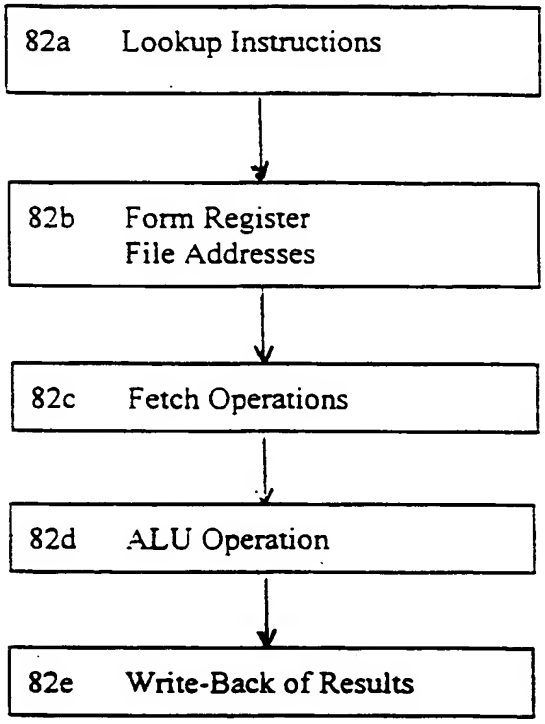
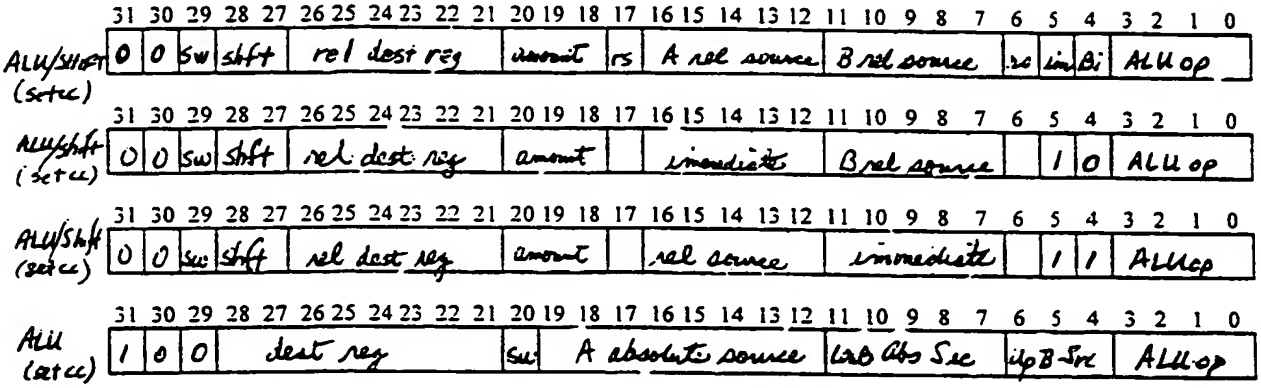

82a Lookup Instructions
82b Form Register File Addresses
82c Fetch Operations
82d ALU Operation
82e Write-Back of Results

FIG. 4



Shift Decode:

(rs, r0) decode ([31:0] shifts into [63:32] and take [63:32]):

00 = left rotate
01 = right shift (32-ShfAmt = Right Shft Amt)
10 = left shift
11 = double shift (upper A-op shifts into lower B-op)

===> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B	0100 = ~A&B (~and)	1000 = A-B	1100 = A+B(8)
0001 = ~B	0101 = XOR	1001 = B-A	1101 = A+B(16)
0010 = A&B (and)	0110 = OR	1010 =	1110 = A+B
0011 = A&~B (and~)	0111 = mul-stuff	1011 =	1111 = A+B+Cin

FIG. 5